FIG. 1

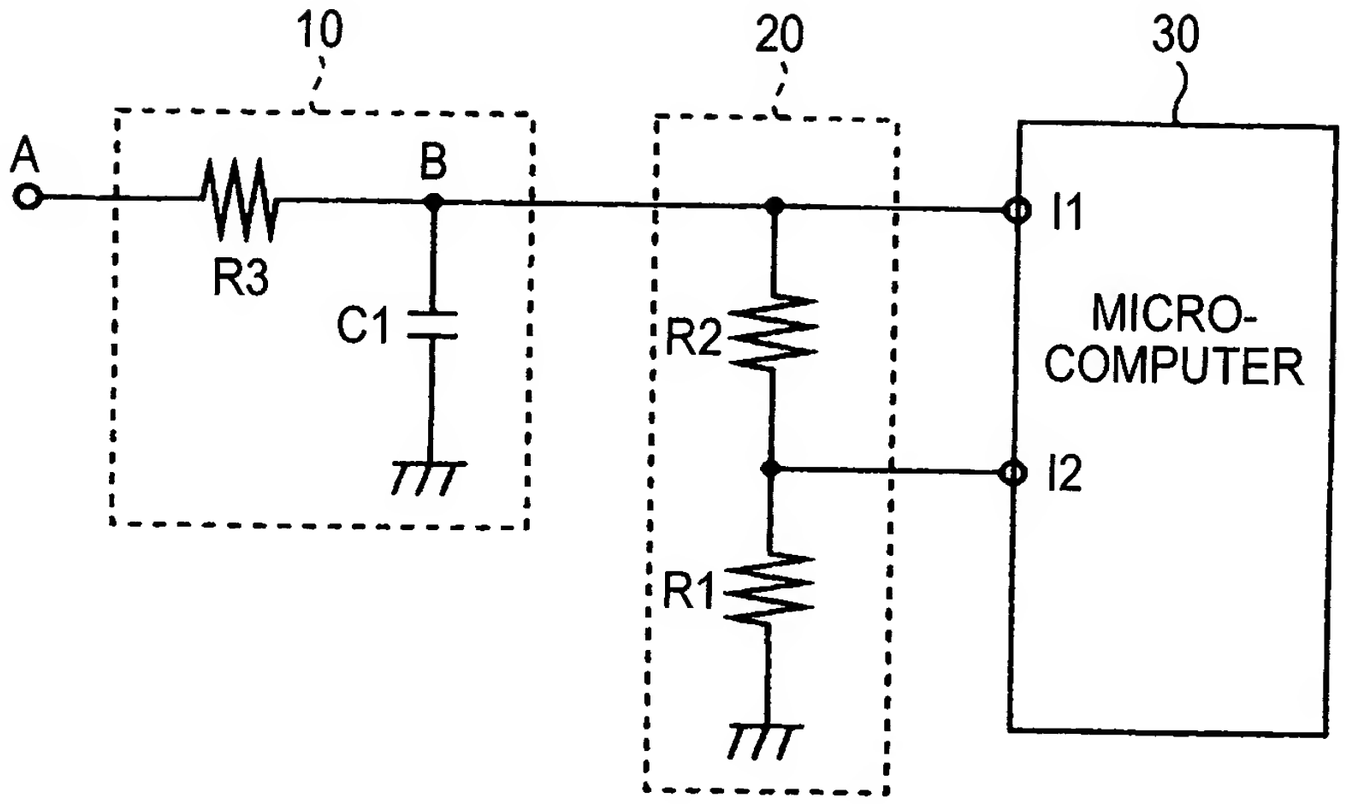

FIG. 2A

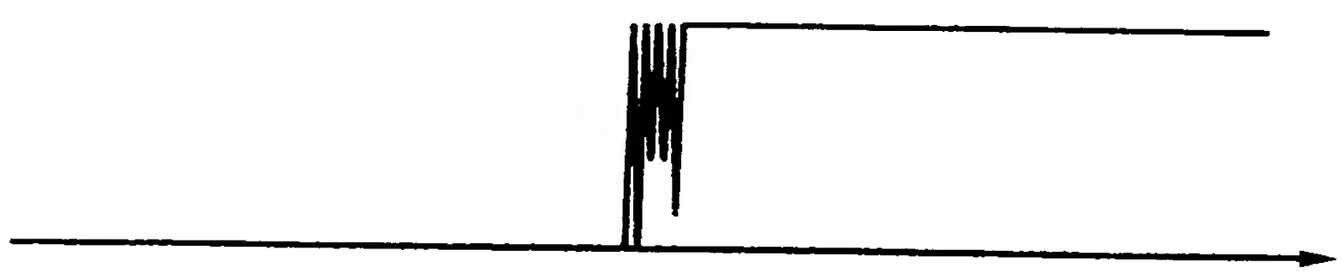

FIG. 2B

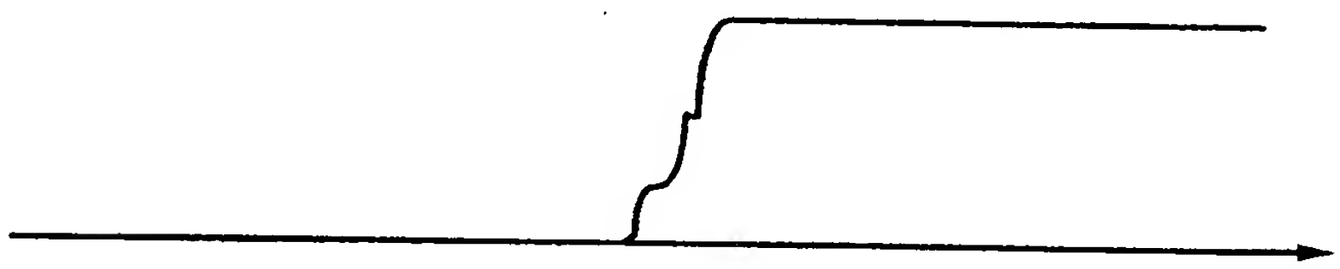

FIG. 3

INPUT VOLTAGE	I1	I2	PROCESS RESULT
$Vi \geqq (1 + R2/R1) \cdot Vth$	Hi	Hi	Hi
$(1 + R2/R1) \cdot Vth > Vi \geqq Vth$	Hi	Lo	UNCHANGED
$Vth > Vi$	Lo	Lo	Lo

FIG. 4A

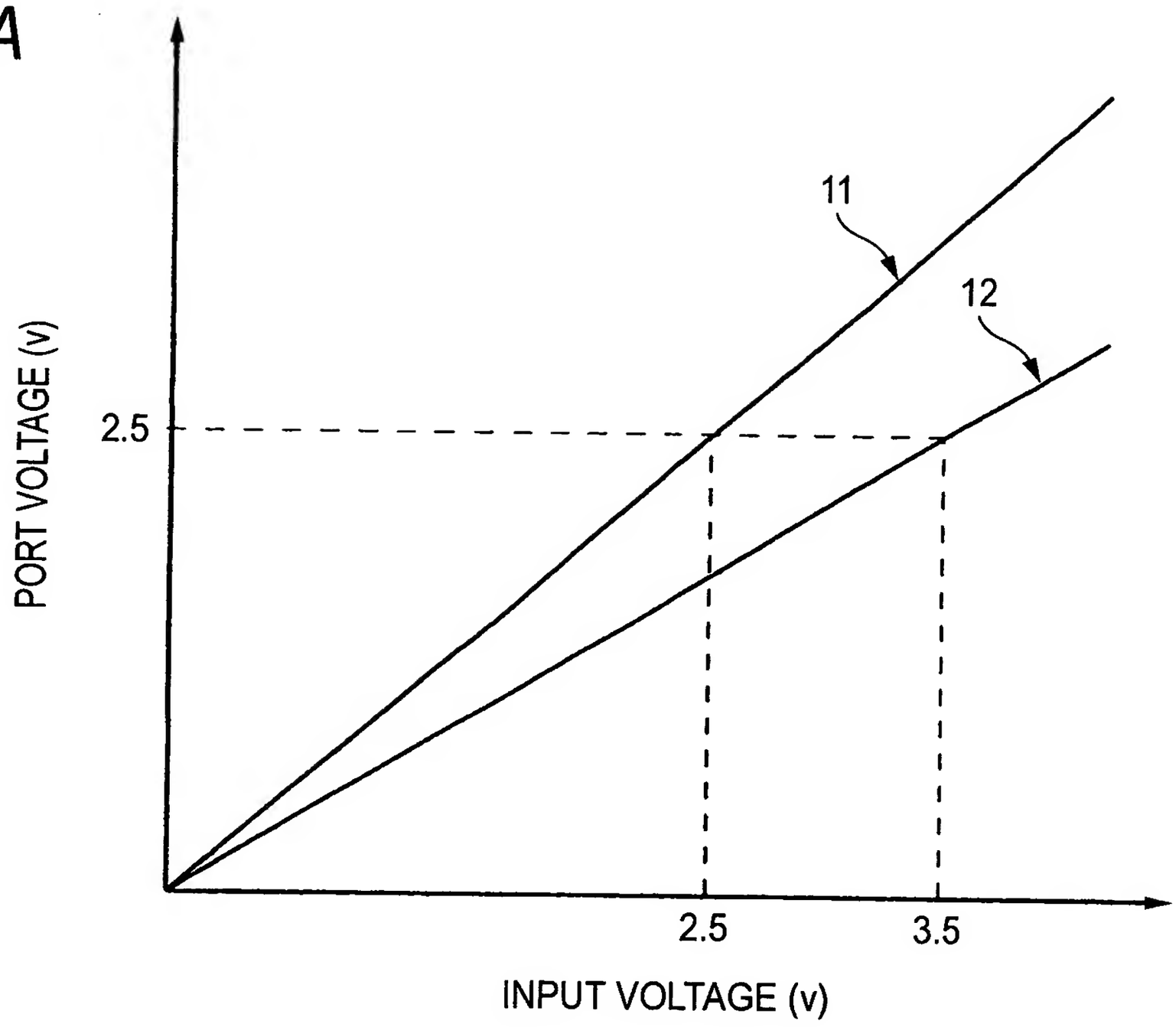

FIG. 4B

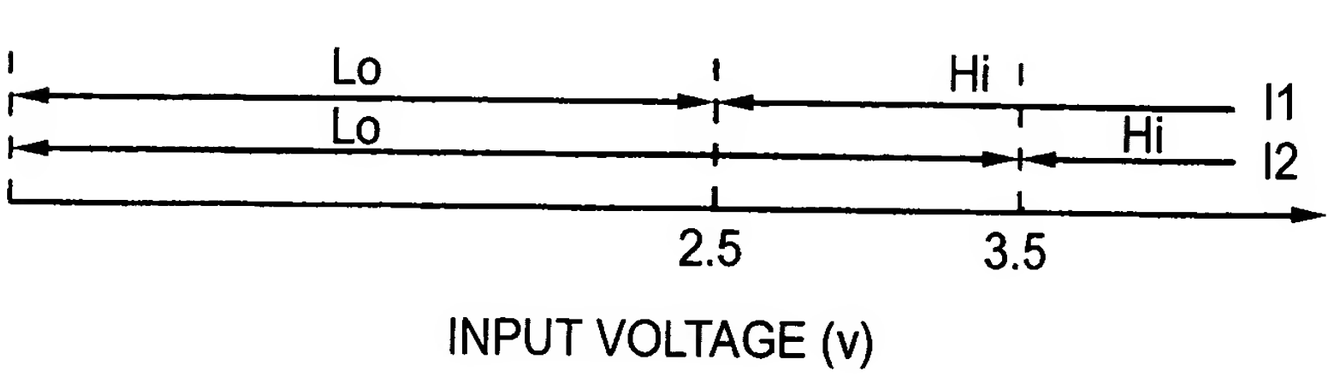

FIG. 4C

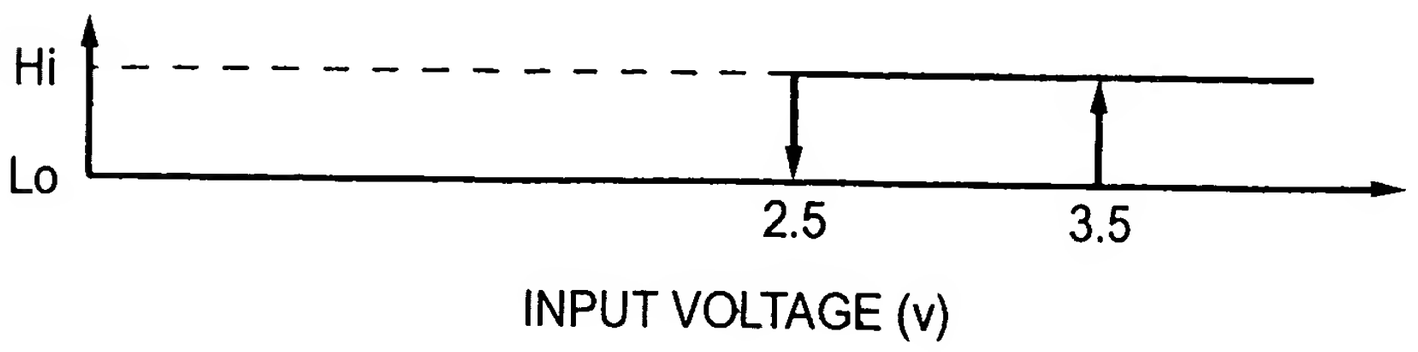

FIG. 5